UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,960	08/07/2003	Clark A. Carty	72255/26765	1231

23380 7590 11/19/2007
TUCKER ELLIS & WEST LLP
1150 HUNTINGTON BUILDING
925 EUCLID AVENUE
CLEVELAND, OH 44115-1414

EXAMINER	
CHAN, SAI MING	
ART UNIT	**PAPER NUMBER**
2616	

NOTIFICATION DATE	DELIVERY MODE
11/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@tuckerellis.com
mary.erne@tuckerellis.com

Office Action Summary	Application No.	Applicant(s)	
	10/635,960	CARTY ET AL.	
	Examiner	Art Unit	
	Sai-Ming Chan	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *7 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-19 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Applicant's Amendment filed 7/28/2007 is acknowledged.
- Claims 1 and 11 have been amended
- Claims 7 to 20 have been cancelled
- Claim 21 is new

Information Disclosure Statement

The information disclosure statement (IDS) submitted on February 25, 2005 has been considered by the Examiner and made of record in the application file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 5-6, 9-11, 15-15 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gillies et al. (U.S.Patent Publication # 20030212821),** in view of **Burgess et al. (U.S. Patent # 7283525),** and further in view of **Boucher et al. (U.S. Patent #6247060).**

Consider **claims 1 and 11, Gillies et al.** clearly disclose and show an application-specific integrated circuit comprising: switch circuitry for receiving a data frame and forwarding it to a predetermined port (fig. 9; abstract, lines 1-2); inspection circuitry for inspecting attributes of the data frame (fig. 2a (70), paragraph 54); decision circuitry for instructing the switch circuitry to forward the data frame based on the attributes (fig. 2a (routing device 30); paragraph 54); a plurality of wireless access points (fig.9 (DC 901, 903, 905 & 907))

However, Gillies et al. do not specifically disclose the ASIC memory mapping interface which stores packets for access points and for MAC to access the packets.

In the same field of endeavor, Burgess et al. clearly show and disclose a memory mapped interface (column 5, lines 1-15 (matching)) in data communication with the ASIC (fig. 1 (ASIC 2a-5a), column 4, lines 11-21);
wherein the memory mapped interface stores packets (column 5, lines 1-15 (packet stored)) provides Media Access Control layer processors (column 4, lines 11-21) with access to the data frames (column 1, lines 55-67):
wherein a data frame is stored in a memory area (fig. 1 (68), column 4, lines 11-21) corresponding to a wireless access point (fig. 9 (81)) for transmitting the packet (column 4, lines 11-21(storage before transmission)).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an integrated circuit, as taught by Gillies et

al., and provide memory and mapping, as taught by Burgess et al, so that packets are associated with the correct port.

However, Gillies et al., as modified by Burgess et al., do not specifically disclose the packets stays in the memory after transmission until a message is received.

In the same field of endeavor, Boucher et al. clearly show and disclose the data frame remaining in the memory area (column 49, lines 45-57 (packet remains in memory until mfreem)) until after the data frame is transmitted (column 49, lines 45-57(passed to the slow-path)) by the wireless access point and an acknowledgement for the data frame is received (column 49, lines 45-57 (packet remains in memory until mfreem)) by a Media Access Control processor (column 12, lines 5-17 (MAC)) associated with the wireless access point.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an integrated circuit, as taught by Gillies et al., provide memory and mapping, as taught by Burgess et al, and demonstrate packets remain in memory after transmission, in order to transmit the data frames efficiently.

Consider **claim 5,** and **as applied to claim 1 above,** Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the integrated circuit further comprising protocol conversion circuitry for translating the data frame between a first protocol and a second protocol (fig. 1 (20), paragraph 48, lines 1-3, lines 10-13; fig. 9 (between wired and wireless)).

Consider **claim 6,** and **as applied to claim 5 above,** Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show integrated circuit wherein the first protocol is an Ethernet network protocol and the second protocol is a wireless protocol (fig. 1(20), paragraph 48, lines 1-3, lines 10-13; fig. 9 (between wired and wireless)).

Consider **claim 9,** and **as applied to claim 1 above,** Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the integrated circuit further comprising circuitry for translating data frames between a first protocol and a second protocol (fig. 1(20), paragraph 48, lines 1-3, lines 10-13; fig. 9 (between wired and wireless)).

Consider **claim 10,** and **as applied to claim 9 above,** Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the integrated circuit wherein the first protocol is an Ethernet network protocol and the second protocol as a wireless protocol (fig. 1(20), paragraph 48, lines 1-3, lines 10-13; fig. 9 (between wired and wireless)).

Consider **claim 15,** and **as applied to claim 11 above,** Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the network switch further comprising protocol conversion circuitry for translating the data frame between a first protocol and a second protocol (fig. 1(20), paragraph 48, lines 1-3, lines 10-13; fig. 9 (between wired and wireless)).

Consider **claim 16,** and **as applied to claim 15 above,** Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the network switch wherein the first protocol is an Ethernet network protocol and the second protocol is a wireless protocol (fig. 1(20), paragraph 48, lines 1-3, lines 10-13; fig. 9 (between wired and wireless)).

Consider **claim 21,** and **as applied to claim 1 above,** Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show 21. The integrated circuit of claim 1, further comprising one of a group consisting of a core for 802.11 (paragraph 0048 (802.11 wireless)) to 802.3 (paragraph 0048(802.3(Ethernet))) header stripping (paragraph 0048(network cariies 802.3 to 802.11 or vice versa, which means header has to converted)), a core for 802.11 to 802.3 encapsulation (fig. 4, paragraph 0031 (encapsulated packet)), a core for providing Message Integrity Check (MIC) (inherently taught in paragraph 0048 (MIC is part of 802.11 standard)) hardware assistance, and radio client association tables (paragraph 0025(routing table)).

Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gillies et al. (U.S.Patent Publication # 20030212821),** in view of **Burgess et al. (U.S. Patent # 7283525),** and in view of **Boucher et al. (U.S. Patent #6247060),** and further in view of **Sinivaara et al. (U.S. Patent # 7020439).**

Consider **claim 2**, as **applied to claim 1 above**, Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show an application-specific integrated circuit as described.

However, Gillies et al., as modified by Burgess et al. and Boucher et al., do not specifically disclose the inspection circuitry which will block data frame from non-wireless ports.

In the same field of endeavor, Sinivaara et al. clearly show and disclose the inspection circuitry is configured to inspect for wireless attributes (fig. 1; column 3,lines 46-52 (mobile terminals)) and wherein the decision circuitry is configured to block non-wireless data frames from wireless ports (fig. 1; column 3, lines 46-52; lines 60-65 (examine the service report to prevent incorrect decision)).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an integrated circuit, as taught by Gillies et al., and provide the inspection and switch circuitries, as taught by Sinivaara et al, in order to transmit the data frames efficiently.

Consider **claim 12**, as **applied to claim 11 above**, Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show an application-specific integrated circuit as described.

However, Gillies et al. do not specifically disclose the inspection circuitry which will block data frame from non-wireless ports.

In the same field of endeavor, Sinivaara et al. clearly show and disclose the inspection circuitry is configured to inspect for wireless attributes (fig. 1; column 3,lines 46-52 (mobile terminals)) and wherein the decision circuitry is configured to block non-wireless data frames from wireless ports (fig. 1; column 3, lines 46-52; lines 60-65 (examine the service report to prevent incorrect decision)).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an integrated circuit, as taught by Rosner et al., and provide the inspection and switch circuitries, as taught by Sinivaara et al, in order to transmit the data frames efficiently.

Claims 3-4, 7-8, 13-14 and 17-19 are rejected under 35 U.S.C. 103(a)

as being unpatentable over **Gillies et al. (U.S. Patent Publication # 20030212821),** in view of **Burgess et al. (U.S. Patent # 7283525),** and in view of **Boucher et al. (U.S. Patent #6247060),** and further in view of **Rosner et al. (U.S. Patent # 7149213).**

Consider **claim 3**, as **applied to claim 1 above**, Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the integrated circuit as described.

However, Gillies et al., as modified by Burgess et al. and Boucher et al., do not specifically disclose the priority involved in data transmission.

In the same field of endeavor, Rosner et al. clearly show and disclose the inspection circuitry is configured to determine whether a data frame is of higher priority (column 8, lines 54-61) than another data frame, and wherein the decision circuitry is configured to grant precedence (column 9, lines 9-13) in forwarding to the higher priority data frame.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an integrated circuit, as taught by Gillies et al., and consider the priority in data transmission, as taught by Rosner et al., in order to transmit the data frames efficiently.

Consider **claim 4**, as **applied to claim 3 above**, Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the integrated circuit as described.

However, Gillies et al., as modified by Burgess et al. and Boucher et al., do not specifically disclose the priority involved in data transmission.

In the same field of endeavor, Rosner et al. clearly show and disclose the integrated circuit further comprising a queue for prioritizing data frames (column 10, lines 1-7), so as to provide quality of service.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an integrated circuit, as taught by Gillies et al., and consider the priority queue in data transmission, as taught by Rosner et al., in order to transmit the data frames efficiently.

Consider **claim 7**, as **applied to claim 1 above**, Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the integrated circuit as described.

However, Gillies et al., as modified by Burgess et al. and Boucher et al., do not specifically disclose the memory map involved in the data transmission.

In the same field of endeavor, Rosner et al. clearly show and disclose the integrated circuit further comprising a memory map (fig. 2 (36); fig. 7 (step 78)) for storing and retrieving data frames in a memory according to a data frame's address.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an integrated circuit, as taught by Gillies et al., and make use of the memory map in data transmission, as taught by Rosner et al., in order to transmit the data frames efficiently.

Consider **claim 8**, as **applied to claim 1 above**, Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the integrated circuit as described.

However, Gillies et al., as modified by Burgess et al. and Boucher et al., do not specifically disclose the priority involved in data transmission.

In the same field of endeavor, Rosner et al. clearly show and disclose the integrated circuit further comprising circuitry for selectively retrieving data frames based on priority (column 11, lines 38-57).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a network switch, as taught by Gillies et al., and make use of the memory map in data transmission, as taught by Rosner et al., in order to transmit the data frames efficiently.

Consider **claim 13**, as **applied to claim 11 above**, Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the network switch as described.

However, Gillies et al., as modified by Burgess et al. and Boucher et al., do not specifically disclose the priority involved in data transmission.

In the same field of endeavor, Rosner et al. clearly show and disclose the inspection circuitry is configured to determine whether a data frame is of higher priority (column 8, lines 54-61) than another data frame, and wherein the decision circuitry is configured to grant precedence (column 9, lines 9-13) in forwarding to the higher priority data frame.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a network switch, as taught by Gillies et al., and consider the priority in data transmission, as taught by Rosner et al., in order to transmit the data frames efficiently.

Consider **claim 14**, as **applied to claim 13 above**, Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the network switch as described.

However, Gillies et al., as modified by Burgess et al. and Boucher et al., do not specifically disclose the priority involved in data transmission.

In the same field of endeavor, Rosner et al. clearly show and disclose the network switch further comprising a queue for prioritizing data frames (column 10, lines 1-7), so as to provide quality of service.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a network switch, as taught by Gillies et al., and consider the priority queue in data transmission, as taught by Rosner et al., in order to transmit the data frames efficiently.

Consider **claim 17**, as **applied to claim 11 above**, Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the network switch as described.

However, Gillies et al., as modified by Burgess et al. and Boucher et al., do not specifically disclose the memory map involved in the data transmission.

In the same field of endeavor, Rosner et al. clearly show and disclose the network switch further comprising a memory map (fig. 2 (36); fig. 7 (step 78)) for storing and retrieving data frames in a memory according to a data frame's address.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a network switch, as taught by Gillies et al., and make use of the memory map in data transmission, as taught by Rosner et al., in order to transmit the data frames efficiently.

Consider **claim 18**, as **applied to claim 17 above**, Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the network switch as described.

However, Gillies et al., as modified by Burgess et al. and Boucher et al., do not specifically disclose the priority involved in data transmission.

In the same field of endeavor, Rosner et al. clearly show and disclose the network switch further comprising circuitry for selectively retrieving data frames based on priority (column 11, lines 38-57).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a network switch, as taught by Gillies et al., and make use of the memory map in data transmission, as taught by Rosner et al., in order to transmit the data frames efficiently.

Consider **claim 19,** and **as applied to claim 17 above,** Gillies et al., as modified by Burgess et al. and Boucher et al., clearly disclose and show the network switch further comprising circuitry for translating data frames between a first protocol and a second protocol (fig. 1(20), paragraph 48, lines 1-3, lines 10-13; fig. 9 (between wired and wireless)).

Response to Arguments

Applicant's arguments filed on July 28, 2007, with respect to claims 1, 11 and 21, on page 7 and through page 8 of the remarks, have been fully considered but they are moot in view of the new ground(s) of rejection necessitated by the new limitations added to claims 1, 11 and 21. See the above rejections of claims 1, 11 and 21 for the relevant interpretation and citations found in Burgess et al. and Boucher et al., disclosing the newly added limitations.

Conclusion

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

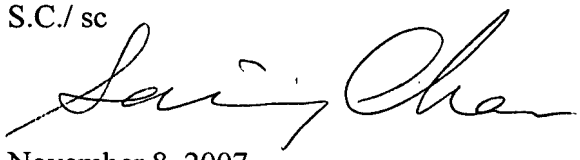
Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Sai-Ming Chan whose telephone number is (571) 270-1769. The Examiner can normally be reached on Monday-Thursday from 6:30am to 5:00pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 571-272-4100.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Sai-Ming Chan
S.C./ sc



November 8, 2007

CHIRAG G. SHAH
PRIMARY PATENT EXAMINER